CLAIMS

What is claimed is:

1. A method to operate a digital signal receiver, comprising:

detecting the occurrence of a symbol degrading event for a received signal;

inserting zero symbols into a received symbol stream prior to de-interleaving the received signal; and

error correction decoding the received symbol stream having the inserted zero symbols.

2. A method as in claim 1, where error correction decoding comprises operating a Reed-Solomon decoder.

3. A method as in claim 1, where error correction decoding comprises operating a BCH decoder.

4. A method as in claim 1, where error correction decoding comprises operating a Turbo decoder.

5. A method as in claim 1, where inserting occurs in conjunction with operating a BPSK bit metric calculator.

6. A method as in claim 1, where inserting occurs after a Viterbi decoder.

7. A method as in claim 1, where error correction decoding comprises first de-interleaving the received symbol stream having the inserted zero symbols.

8. A method as in claim 1, where detecting comprises:

estimating a signal to noise ratio (SNR) of a block of L contiguous received symbols;

comparing the estimated SNR to a threshold SNR value; and

replacing L symbols with L zero symbols when the estimated SNR is less than the threshold SNR.

9. A method as in claim 1, where detecting comprises examining the output of at least one Automatic Gain Control (AGC) circuit.

10. A method as in claim 9, where detecting comprises comparing the output of a slow AGC to a first threshold, comparing the output of a fast AGC to a second threshold, and replacing symbols with zero symbols when either the first or the second threshold is exceeded.

11. A method as in claim 9, where detecting comprises comparing a difference between the output of a slow AGC and the output of a fast AGC to a threshold, and replacing symbols with zero symbols when the difference exceeds the threshold.

12. A method as in claim 9, where detecting comprises comparing a difference between the output of a fast AGC and an average of the output of the fast AGC to a threshold, and replacing symbols with zero symbols when the difference exceeds the threshold.

13. A method as in claim 1, where detecting uses information received from a transmitter that is indicative of a time when a deep fade occurs.

14. A digital signal receiver, comprising:

circuitry for detecting the occurrence of a symbol degrading event for a received signal and for inserting zero symbols into a received symbol stream prior to de-interleaving the received signal; and

a decoder for decoding the received symbol stream having the inserted zero symbols.

15. A digital signal receiver as in claim 14, where the decoder comprises a Reed-Solomon decoder.

16. A digital signal receiver as in claim 14, where the decoder comprises a BCH decoder.

17. A digital signal receiver as in claim 14, where the decoder comprises a Turbo decoder.

18. A digital signal receiver as in claim 14, where said circuit inserts the zero symbols in conjunction with operation of a BPSK bit metric calculator.

19. A digital signal receiver as in claim 14, where said circuit inserts the zero symbols after a Viterbi decoder.

20. A digital signal receiver as in claim 14, further comprising a de-interleaver for de-interleaving the received symbol stream having the inserted zero symbols.

21. A digital signal receiver as in claim 14, where said circuit comprises:

means for estimating a signal to noise ratio (SNR) of a block of L contiguous received symbols;

means for comparing the estimated SNR to a threshold SNR value; and

means for replacing L symbols with L zero symbols when the estimated SNR is less than the threshold SNR.

22. A digital signal receiver as in claim 14, where said circuit comprises means for examining the output of at least one Automatic Gain Control (AGC) circuit.

23. A digital signal receiver as in claim 22, where said circuit comprises means for comparing the output of a slow AGC to a first threshold, means for comparing the output of a fast AGC to a second threshold, and means for replacing symbols with zero symbols when either the first or the second threshold is exceeded.

24. A digital signal receiver as in claim 22, where said circuit comprises means for comparing a difference between the output of a slow AGC and the output of a fast AGC to a threshold, and means for replacing symbols with zero symbols when the difference exceeds the threshold.

25. A digital signal receiver as in claim 22, where said circuit comprises means for comparing a difference between the output of a fast AGC and an average of the output of the fast AGC to a threshold, and means for replacing symbols with zero symbols when the difference exceeds the threshold.

26. A digital signal receiver as in claim 14, where said circuit uses information received from a transmitter that is indicative of a time when a deep fade occurs.

27. A method to receive a signal that passes through a channel that is periodically obstructed by a rotating propeller blade, comprising:

detecting the occurrence of a fading condition due to obstruction by the propeller blade;

in response to detecting the occurrence of the fading condition, inserting zero symbols into a received symbol stream at the receiver;

de-interleaving the received symbol stream having the inserted zero symbols; and

decoding the received symbol stream having the inserted zero symbols.

28. A method as in claim 27, where decoding comprises operating a concatenated forward error correction (FEC) decoder.

29. A method as in claim 27, where decoding comprises operating one of a Reed-Solomon decoder, a BCH decoder, or a Turbo decoder.

30. A method to operate a satellite to receive a signal that passes through a channel that is periodically obstructed by a rotating propeller blade, comprising:

detecting, on the satellite, the occurrence of a fading condition due to obstruction by the propeller blade;

in response to detecting the occurrence of the fading condition, inserting zero symbols into a received symbol stream at the satellite;

de-interleaving the received symbol stream having the inserted zero symbols; and

error correction decoding the received symbol stream having the inserted zero symbols.

31. A satellite, comprising a receiver for receiving a signal that passes through a channel that is periodically obstructed, the receiver comprising circuitry for detecting the occurrence of a fading condition due to an obstruction and, in response to detecting the occurrence of the fading condition, for inserting zero symbols into a received symbol stream; and an error correction decoder for decoding the received symbol stream having the inserted zero symbols.